2015/10/13

Product Brief

JESD204B TX/RX IP CORE

Product Overview

KuanTek JESD204B IP Core implements JEDEC's JESD204B standard. JESD204B is a high speed serial communication interface between ADC or DAC devices and logic device. Number of lanes of the core can be configured from 1 to 8 by the provided synthesis scripts (RTL License). It can be configured on microprocessor by AXI4-Lite protocol. The JESD204B IP Core can be used as a receiver or a transmitter and can perform scrambling, descrambling, alignment character insertion and replacement, frame and lane alignment. It also supports the test modes in JEDEC's JESD204B standard (RPAT, JSPAT etc.).

Hardware Architecture

The receiver IP Core receives ADC data via multi gigabit transceivers of the FPGA device. Then data are decoded on 8B/10B decoding module. Decoded data are synchronized according to initial frame and initial lane based on the subclass version. Synchronized data pass through self-synchronous descrambler module with the following polynomial $1 + x^{14} + x^{15}$.

First the transmitter IP Core sends data which is being received via AXI4-Stream interface or test sequence to scrambler module which implements the following polynomial $1 + x^{14} + x^{15}$. During this process the IP inserts appropriate frame or lane alignment characters into the data stream. Then the entire stream is encoded according to 8B/10B coding standard. Finally the 8B/10B encoded data package is transmitted via multi gigabit transceivers of the FPGA device.

Features

- Compatible with JEDEC JESD204B Standard (JESD204B.01, 2012)
- Lane speeds up to 12.5 Gbits/s (Device dependent)
- AMBA-AXI4-Lite Configuration Interface (32-bits)
- AMBA-AXI4-Stream Data Interface(32-bits)
- Configurable between 1 to 8 lanes
- Subclass 0,1,2 Support
- Initial lane alignment support
- Scrambling and Descrambling
- Lane synchronization support
- Runtime configurable F and K parameters
- 8B/10B Coding available upon request

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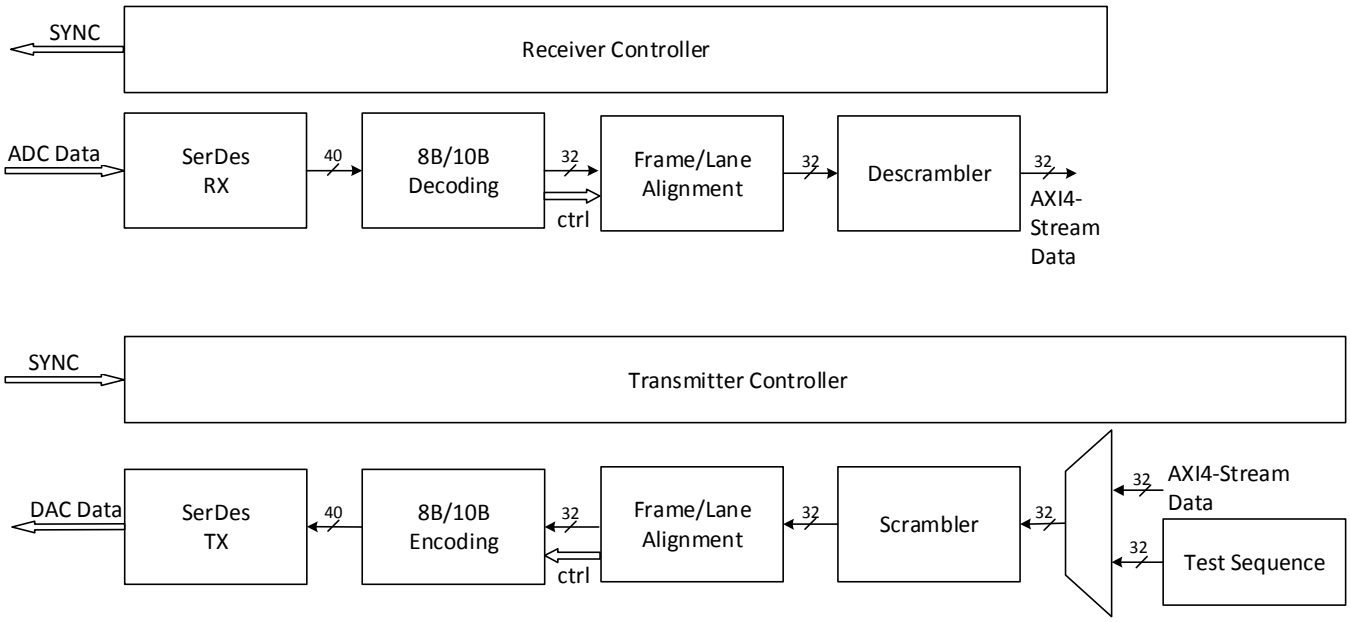

Software Interface

The JESD204B IP Core can be configured by a microprocessor via AXI4-Lite interface. It has a register map for configuration parameters such as octets per frame, frame per multi-frame, subclass, enabling scrambling/descrambling functionality, lengths of initial lane alignment sequence etc. The configuration data stored in the register map can be both changed or observed via the AXI-Lite interface.

Verification

The JESD204B IP Core's functionality has been intensively verified by using object oriented approach thanks to SystemVerilog. Both stimuli and configuration data is generated randomly until specific coverage points are reached (Constrained Random Verification). Assertions are intensively used by both design and verification teams.

Deliverables

- Verilog RTL source codes (RTL License)
- Netlist file for Xilinx FPGAs (FPGA Netlist License)
- User manual
- Test bench
- Optional integration support
- Optional Requirements Traceability Matrix for DO-254 Certification
- Optional Hardware Requirements Document
- Optional Conceptual Design Document
- Optional Test Plan Document

Related Product Codes: KNTK-IP-JESD204B-TX-100, KNTK-IP-JESD204B-RX-100

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